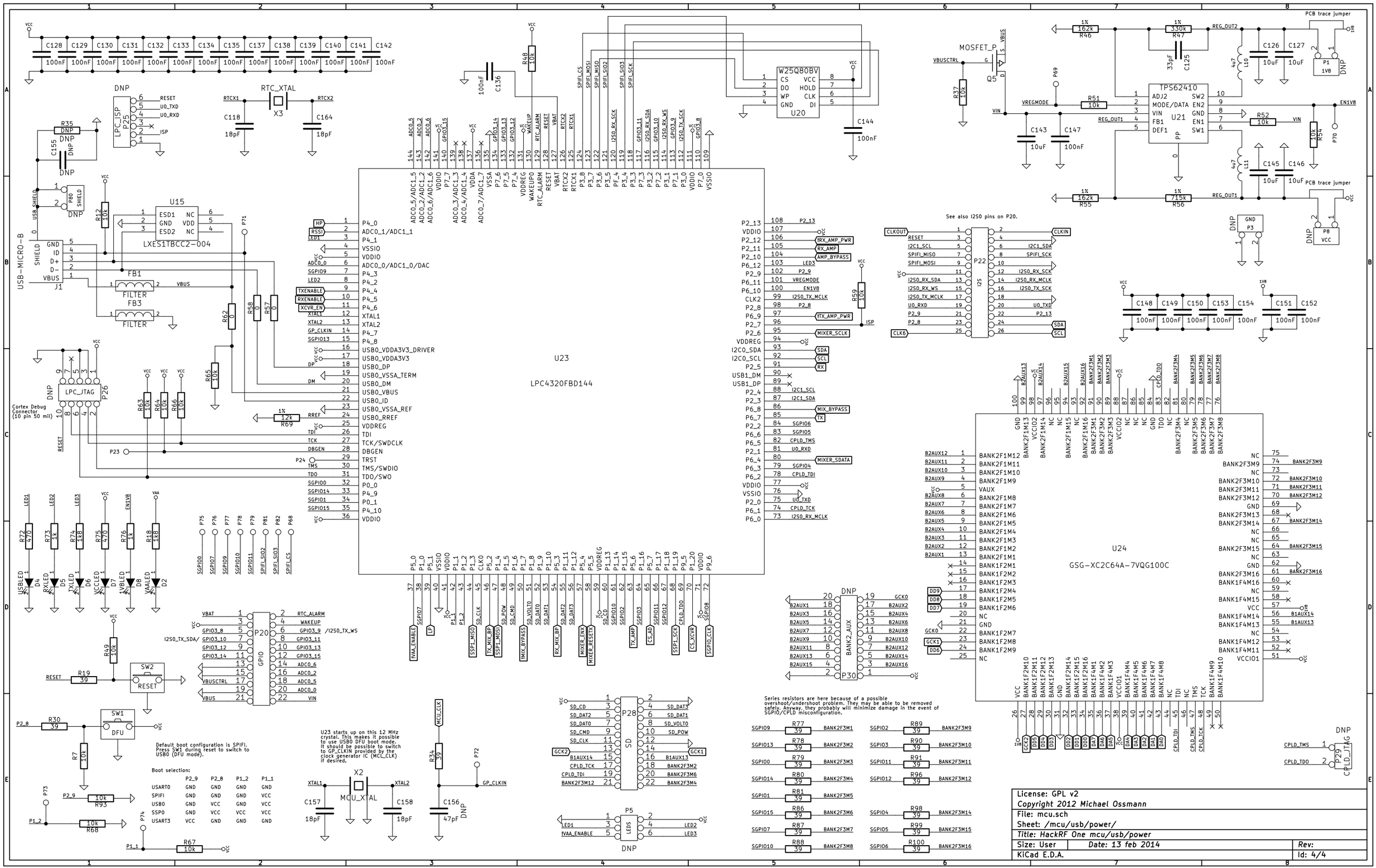
C128 C129 C130 C131 C132 C133 C134 C135 C137 C138 C139 C140 C141 C142
100nF
DNP
LPC_ISP
P25
RESET
U0_TXD
U0_RXD
ISP
RTC_XTAL
X3
RTCX1
RTCX2
C118
18pF
C164
R35
C155
USB-MICRO-B
J1
USB_SHIELD
PBO SHIELD
U15
LXES1TBCC2-004
ESD1
ESD2
GND
VDD
NC
FB1
FB3
FILTER
VBUS
R12
R62
R58
R57
R65
R63
R64
R66
LPC_JTAG
P26
Cortex Debug Connector (10 pin 50 mil)
R69
12k
RREF
P23
P24
TMS
TDI
TCK
DBGEN
TRST
TDO
R48
C136
W25Q80BV
U20
SPIFI_CS
SPIFI_MOSI
SPIFI_MISO
SPIFI_SIO2
SPIFI_SIO3
SPIFI_SCK
C144
U23
LPC4320FBD144
P4_0
P4_1
P4_2
P4_3
P4_4
P4_5
P4_6
P4_7
P4_8
P4_10
P0_0
P0_1
P0_2
P0_3
P0_4
P0_5
P0_6
P0_7
P1_0
P1_1
P1_2
P1_3
P1_4
P1_5
P1_6
P1_7
P1_8
P1_9
P1_10
P1_11
P1_12
P1_13
P1_14
P1_15
P1_16
P1_17
P1_18
P1_19
P1_20
P2_0
P2_1
P2_2
P2_3
P2_4
P2_5
P2_6
P2_7
P2_8
P2_9
P2_10
P2_11
P2_12
P2_13
P3_0
P3_1
P3_2
P3_3
P3_4
P3_5
P3_6
P3_7
P3_8
P4_9
P5_0
P5_1
P5_2
P5_3
P5_4
P5_5
P5_6
P5_7
P6_0
P6_1
P6_2
P6_3
P6_4
P6_5
P6_6
P6_7
P6_8
P6_9
P6_10
P6_11
P6_12
P7_0
P7_1
P7_2
P7_3
P7_4
P7_5
P7_6
P7_7
P8_0
P8_1
P8_2
P8_3
P8_4
P8_5
P8_6
P8_7
P9_5
P9_6
USB0_VDDA3V3_DRIVER
USB0_VDDA3V3
USB0_DP
USB0_VSSA_TERM
USB0_DM
USB0_VBUS
USB0_ID
USB0_VSSA_REF
USB0_RREF
VDDREG
TDI
TCK/SWDCLK
DBGEN
TRST
TMS/SWDIO
TDO/SWO
VDDIO
VSSIO
XTAL1
XTAL2
RTC_ALARM
WAKEUP
RESET
VBAT
ADC0_0/ADC1_0/DAC
ADC0_1/ADC1_1
ADC0_2/ADC1_2
ADC0_3/ADC1_3
ADC0_4/ADC1_4
ADC0_5/ADC1_5
ADC0_6/ADC1_6
ADC0_7/ADC1_7
VDDA
VSSA
VDDREG
VDDIO
VSSIO
I2C0_SCL
I2C0_SDA
USB1_DP
USB1_DM
CLK2
VREGMODE
EN1V8
I2S0_TX_MCLK
I2S0_RX_SCK
I2S0_RX_WS
I2S0_RX_SDA
I2S0_TX_SCK
GPIO3_15
GPIO3_14
GPIO3_13
GPIO3_12
GPIO3_11
GPIO3_10
GPIO3_9
GPIO3_8
GPIO0_8
GPIO0_9
GPIO0_10
GPIO0_11
GPIO1_8
GPIO1_9
GPIO1_10
GPIO1_11
GPIO1_12
GPIO1_13
GPIO1_14
GPIO1_15
HP
RSSI
LED1
LED2
LED3
ADC0_0
SGPIO9
TXENABLE
RXENABLE
XCVR_EN
XTAL1
XTAL2
GP_CLKIN
SGPIO13
DP
DM
TDI
TCK
DBGEN
TRST
TMS
TDO
SGPIO0
SGPIO14
SGPIO1
SGPIO15
RTCX1
RTCX2
VBAT
RESET
WAKEUP
RTC_ALARM
VDDREG
VSSA
VDDIO
VSSIO
P71
P72
P73
P74
P75
P76
P77
P78
P79
P81
P82
P68
P69
P70
SW1
DFU
SW2
RESET
R30
R7
R19
R49
R93
R68
R67
Default boot configuration is SPIFI.
Press SW1 during reset to switch to USB0 (DFU mode).
Boot selection:
USART0 GND GND GND GND
SPIFI GND GND GND VCC
USB0 GND VCC GND VCC
SSP0 GND VCC VCC VCC
USART3 VCC GND GND GND
P2_9 P2_8 P1_2 P1_1
U23 starts up on this 12 MHz crystal. This makes it possible to use USB0 DFU boot mode. It should be possible to switch to GP_CLKIN provided by the clock generator IC (MCL_CLK) if desired.
X2
MCU_XTAL
C157
18pF
C158
18pF
MCU_CLK
R34
39
C156
47pF
DNP
P20
GPIO
VBAT
WAKEUP
GPIO3_8
GPIO3_10
GPIO3_12
GPIO3_14
VBUSCTRL
VBUS
RTC_ALARM
GPIO3_9
GPIO3_11
GPIO3_13
GPIO3_15
ADC0_6
ADC0_2
ADC0_5
ADC0_0
VIN
I2S0_TX_SDA/
/I2S0_TX_WS
P28
SD
SD_CD
SD_DAT2
SD_DAT0
SD_CMD
SD_CLK
SD_DAT3
SD_DAT1
SD_VOLT0
SD_POW
B1AUX14
CPLD_TDI
BANK2F3M12
GCK2
GCK1
BANK2F3M2
BANK2F3M3
BANK2F3M6
BANK2F3M4
P5
LEDS
LED1
IVAA_ENABLE
LED2
LED3
DNP
USBLED
RXLED
TXLED
VCCLED
1V8BLED
VAALED
D4
D5
D6
D7
D8
D2
R72 470
R73 1k
R74 148
R75 470
R76 1k
R18 148
EN1V8
VAA
P22
I2S
CLKOUT
RESET
I2C1_SCL
SPIFI_MISO
SPIFI_MOSI
I2S0_RX_SDA
I2S0_RX_WS
I2S0_TX_MCLK
U0_RXD
P2_9
P2_8
CLK6
CLKIN
I2C1_SDA
SPIFI_SCK
I2S0_RX_SCK
I2S0_RX_MCLK
I2S0_TX_SCK
U0_TXD
P2_13
SDA
SCL
See also I2S0 pins on P20.
P30
B2AUX_AUX
DNP
B2AUX1
B2AUX3
B2AUX5
B2AUX7
B2AUX9
B2AUX11
B2AUX13
B2AUX15
B2AUX2
B2AUX4
B2AUX6
B2AUX8
B2AUX10
B2AUX12
B2AUX14
B2AUX16
GCK0
GCK1
DD6
DD7
DD8
DD9
U24
GSG-XC2C64A-7VQG100C
BANK2F1M12
BANK2F1M11
BANK2F1M10
BANK2F1M9
VAUX
BANK2F1M8
BANK2F1M7
BANK2F1M6
BANK2F1M5
BANK2F1M4
BANK2F1M3
BANK2F1M2
BANK2F1M1
BANK1F2M1
BANK1F2M2
BANK1F2M3
BANK1F2M4
BANK1F2M5
BANK1F2M6
BANK1F2M7
BANK1F2M8
BANK1F2M9
BANK1F2M10
BANK1F2M11
BANK1F2M12
BANK1F2M13
BANK1F2M14
BANK1F2M15
BANK1F2M16
BANK1F4M1
BANK1F4M2
BANK1F4M3
BANK1F4M4
BANK1F4M5
BANK1F4M6
BANK1F4M7
BANK1F4M8
BANK1F4M9
BANK1F4M10
BANK1F4M11
BANK1F4M12
BANK1F4M13
BANK1F4M14
BANK1F4M15
BANK1F4M16
BANK2F3M1
BANK2F3M2
BANK2F3M3
BANK2F3M4
BANK2F3M5
BANK2F3M6
BANK2F3M7
BANK2F3M8
BANK2F3M9
BANK2F3M10
BANK2F3M11
BANK2F3M12
BANK2F3M13
BANK2F3M14
BANK2F3M15
BANK2F3M16
B2AUX1
B2AUX2
B2AUX3
B2AUX4
B2AUX5
B2AUX6
B2AUX7
B2AUX8
B2AUX9
B2AUX10
B2AUX11
B2AUX12
B2AUX13
B2AUX14
B2AUX15
B2AUX16
CPLD_TDO
CPLD_TMS
CPLD_TCK
CPLD_TDI
P29
CPLD_JTAG
Series resistors are here because of a possible overshoot/undershoot problem. They may be able to be removed safely. Anyway, they probably will minimize damage in the event of SGPIO/CPLD misconfiguration.
SGPIO9 R77 39 BANK2F3M1
SGPIO13 R78 39 BANK2F3M2
SGPIO0 R79 39 BANK2F3M3
SGPIO14 R80 39 BANK2F3M4
SGPIO1 R81 39 BANK2F3M5
SGPIO15 R86 39 BANK2F3M6
SGPIO7 R87 39 BANK2F3M7
SGPIO10 R88 39 BANK2F3M8
SGPIO2 R89 39 BANK2F3M9
SGPIO3 R90 39 BANK2F3M10
SGPIO11 R91 39 BANK2F3M11
SGPIO12 R96 39 BANK2F3M12
SGPIO4 R98 39 BANK2F3M14
SGPIO5 R99 39 BANK2F3M15
SGPIO6 R100 39 BANK2F3M16
MOSFET_P
Q5
VBUSCTRL
R37 10k
TPS62410
U21
ADJ2
MODE/DATA
VIN
FB1
DEF1
SW2
EN2
GND
EN1
SW1
PP
VREGMODE
R51 10k
REG_OUT1
REG_OUT2
R52 10k
R54 10k
R46 162k
R47 330k
33pF C125
R55 162k
R56 715k
C143 10uF
C147 100nF
C126 10uF
C127 10uF
C145 10uF
C146 10uF
4u7 L10
4u7 L11
PCB trace jumper
P1 1V8
P8 VCC
P3 GND
C148 C149 C150 C153 C154 100nF
C151 C152 100nF
License: GPL v2
Copyright 2012 Michael Ossmann
File: mcu.sch
Sheet: /mcu/usb/power/
Title: HackRF One mcu/usb/power
Size: User
Date: 13 feb 2014
Rev:
KiCad E.D.A.
Id: 4/4

C84 22pF, C85 22pF, C86 22pF, C87 10nF, C89 10nF, C90 100pF, C91 100nF, C92 10nF, C93 10nF, C94 22pF

C88 10nF

C71 100nF, C72 2.2uF, C73 100nF, C74 2.2uF, C75 100nF, C76 2.2uF, C77 100nF, C78 2.2uF, C79 100nF, C80 2.2uF, C81 100nF, C82 2.2uF, C83 100nF

C167 100nF, R11 10k, MOSFET_P Q3, VAA_ENABLE, FILTER FB2, PCB trace jumper, C105 10uF, P36 DNP

test points: P37 SCL, P38 SDA, P39 SSP1_SCK, P40 SSP1_MOSI, P41 SSP1_MISO, P53 CS_XCVR, P54 CS_AD, P55 TXENABLE, P56 RXENABLE, P57 XTAL2, P58 GCK1, P59 GCK2, P60 SGPIO_CLK, P61 DA0, P62 DA4, P63 DA7, P66 DD0, P64 DD5, P67 DD9, P83 RSSI, P84, P85, P86, P87, P88, P89, P90, P91, P92

RX_IF, RX_BALUN T3, L6 DNP, C99 DNP 22pF, L7 6.2nH, C102 22pF

TX_IF, TX_BALUN T4, L8 DNP, C104 3pF, L9 DNP, C111 3pF

U17 MAX2837

0	EP		
1	VCCRXLNA		
2	GNDRXLNA		
3	B5		
4	RXRF+		
5	RXRF−		
6	B4		
7	VCCTXPAD		
8	B3		
9	B2		
10	TXRF+		
11	TXRF−		
12	B1		
13	VCCTXMX		
14	PABIAS		
15	SCLK	SSP1_SCK	
16	CLOCKOUT	XCVR_CLKOUT	
17	XTAL2	XTAL2	
18	XTAL1		
19	VCCXTAL		
20	VCCDIG		
21	VCCCP		
22	GNDCP		
23	CPOUT+	CPOUT+	
24	CPOUT−	CPOUT−	
25	ENABLE	XCVR_EN	
26	GNDVCO		
27	BYPASS		
28	VCCVCO		
29	DOUT	SSP1_MISO	
30	CS	CS_XCVR	
31	DIN	SSP1_MOSI	
32	RSSI	RSSI	
33	B7		
34	B6		
35	RXBBQ−	RXBBQ−	
36	RXBBQ+	RXBBQ+	
37	RXBBI−		
38	RXBBI+		
39	VCCRXVGA		
40	RXHP		
41	VCCRXFL		
42	TXBBI−		
43	TXBBI+		
44	TXBBQ+		
45	TXBBQ−		
46	VCCRXMX		
47	TXENABLE	TXENABLE	
48	RXENABLE	RXENABLE	

TXBBQ−, TXBBQ+, TXBBI+, TXBBI−, RXBBI+, RXBBI−

C106 1uF, R41 10k

R20 0, R21 0, R22 0, R23 0

C95 DNP 22pF, C96 DNP 22pF

R8 1% 1k QD+, R9 1% 1k QD−, R10 1% 1k ID−, R13 1% 1k ID+

R14 1% 4k7, R15 1% 4k7, R16 1% 4k7, R17 1% 4k7

C97 330nF COM, C98 330nF REFN

C100 330nF

C101 DNP 22pF, C103 DNP 22pF, C107 DNP 22pF, C108 DNP 22pF, C109 DNP 22pF, C110 DNP 22pF

U18 MAX5864

0	EP		
1	REFP	REFP	
2	VDD		
3	IA+	IA+	
4	IA−	IA−	
5	GND		
6	CLK	GCK1	
7	GND		
8	VDD		
9	QA−	QA−	
10	QA+	QA+	
11	VDD		
12	GND		
13	DA0	DA0	
14	DA1	DA1	
15	DA2	DA2	
16	DA3	DA3	
17	OGND		
18	OVDD		
19	DA4	DA4	
20	DA5	DA5	
21	DA6	DA6	
22	DA7	DA7	
23	DD0	DD0	
24	DD1	DD1	
25	DD2	DD2	
26	DD3	DD3	
27	DD4	DD4	
28	DD5	DD5	
29	DD6	DD6	
30	DD7	DD7	
31	DD8	DD8	
32	DD9	DD9	
33	VDD		
34	SSP1_MOSI	SSP1_MOSI	
35	SSP1_SCK	SSP1_SCK	
36	CS_AD	CS_AD	
37	GND		
38	NC		
39	VDD		
40	QD+		
41	GND		
42	VDD		
43	ID−		
44	ID+		
45	REFIN		
46	COM		
47	REFN		
48	REFN		

U19 SI5351C

0	GND		
1	XA	XA	
2	XB	XB	
3	INTR	INTR	
4	SCL	SCL	
5	SDA	SDA	
6	CLKIN	CLKIN	
7	OEB	OEB	
8	CLK3	CLK3	
9	CLK2	CLK2	
10	VDDOB		
11	VDDOA		
12	CLK1	CLK1	
13	CLK0	CLK0	
14	VDDOD		
15	CLK7	MCU_CLK	
16	CLK6	CLK6	
17	CLK5	CLK5	
18	VDDOC		
19	CLK4	MIX_CLK	
20	VDD		

C113 100nF, C115 33pF, C116 47pF

C169 DNP, C170 DNP, X1 GSG-XTAL4PIN

R18 10k R27, R28 10k R104

R31 39 GCK1, R32 39 GCK2, R94 39 SGPIO_CLK, R33 39 CLKOUT

C68 DNP 100pF, C69 DNP 100pF, C159 DNP 100pF, C165 DNP 100pF

P15 INTR, SCL, SDA

P16 CLKIN, 3.3 V CMOS clock input at 10 MHz (or 10 MHz to 100 MHz with firmware modification)

D3 GSG-DIODE-TVS-BI, R85 10k

CLK0 is at the sample rate
CLK1 is at sample rate x2
CLK2 is at sample rate x2

P2 CLKOUT, D9 GSG-DIODE-TVS-BI, R105 10k, P18

3.3 V CMOS clock output at 10 MHz (or other frequency with firmware modification)

C119 100nF, C120 100nF, C121 100nF, C122 100nF

R25 475 180pF C112, R26 475 3.3nF C114

SSP1_MISO, C168 DNP 100pF

P9 BASEBAND: RXBBI−, RXBBI+, TXBBQ+, TXBBQ−, RXBBQ−, RXBBQ+, TXBBI−, TXBBI+

C123 100nF, C124 2.2uF

License: GPL v2	
Copyright 2012 Michael Ossmann	
File: baseband.sch	
Sheet: /baseband/	
Title: HackRF One baseband	
Size: User	*Date: 13 feb 2014* — Rev:
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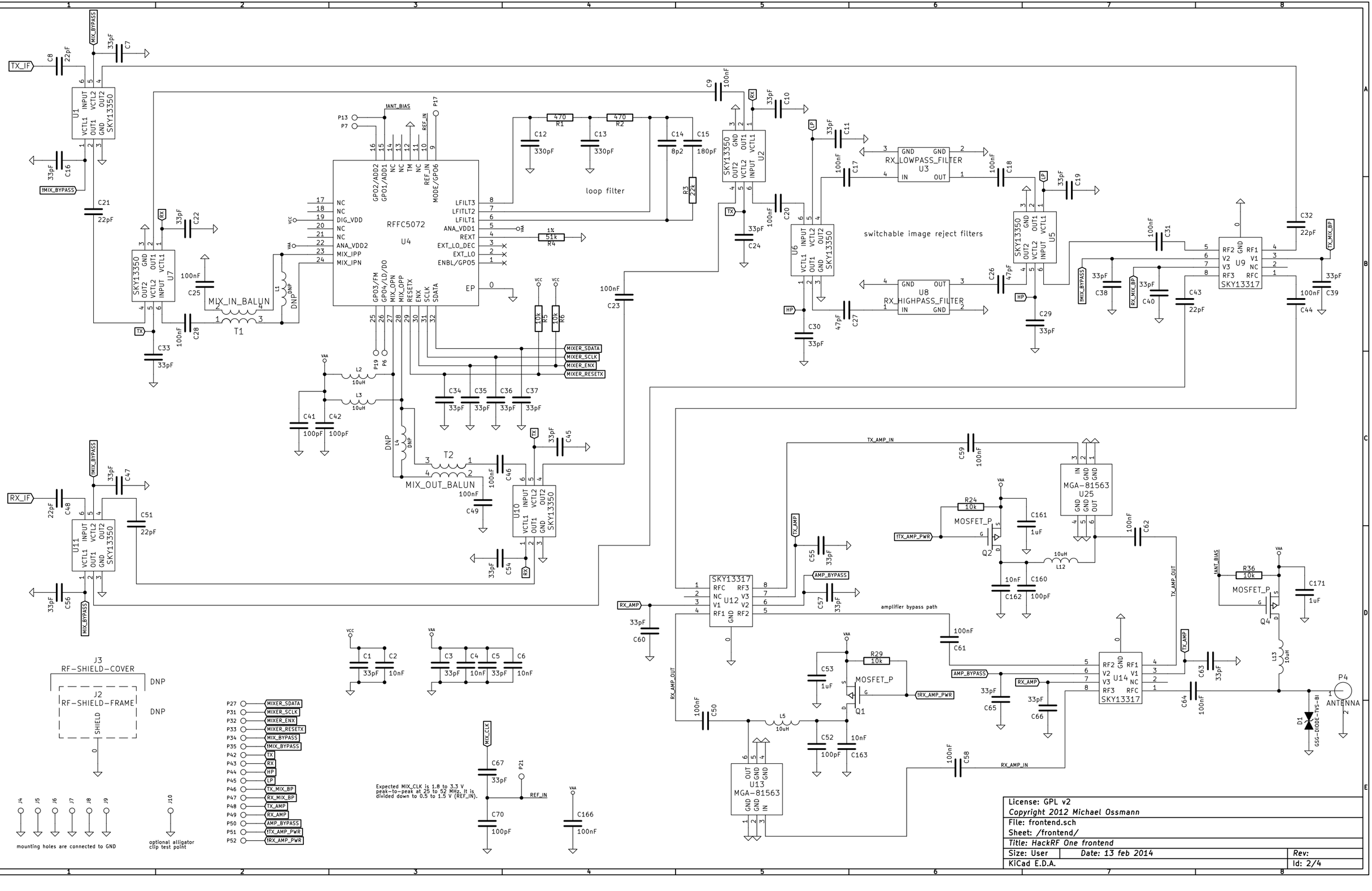
TX_IF
RX_IF
MIX_BYPASS
!MIX_BYPASS
RFFC5072
U4
MIX_IN_BALUN
T1
MIX_OUT_BALUN
T2
loop filter
switchable image reject filters
RX_LOWPASS_FILTER
RX_HIGHPASS_FILTER
SKY13350
SKY13317
MGA-81563
MOSFET_P
TX_AMP_IN
TX_AMP_OUT
RX_AMP_OUT
RX_AMP_IN
amplifier bypass path
ANTENNA
MIXER_SDATA
MIXER_SCLK
MIXER_ENX
MIXER_RESETX
Expected MIX_CLK is 1.8 to 3.3 V peak-to-peak at 25 to 52 MHz. It is divided down to 0.5 to 1.5 V (REF_IN).
mounting holes are connected to GND
optional alligator clip test point
License: GPL v2
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File: frontend.sch
Sheet: /frontend/
Title: HackRF One frontend
Size: User
Date: 13 feb 2014
Rev:
KiCad E.D.A.
Id: 2/4